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EXAMINER	
KO, DANIEL BOKMIN	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,045	BONO, JEAN-PIERRE	
	Examiner	Art Unit	
	Daniel B. Ko	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to the Amendment filed on 7/18/2006.

Any objections and rejections from the prior correspondence not restated in this communication is/are withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1, 4-7, 9, and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over "PAE36 and Linux Virtual Memory System" (www.prism.gatech.edu, printed 12/5/2003), hereinafter simply PAE36, in view of Emmes (U.S. Patent 6,981,125 B2).

Regarding claim 1, PAE36 teaches a digital computer including at least one processor producing virtual addresses over a range of virtual addresses, a translation buffer coupled to said at least one processor for translating the virtual addresses to physical addresses, and a random access memory coupled to the translation buffer for addressing by the physical addresses and coupled to said at least one processor for supplying data to said at least one processor, wherein the random access memory contains physical memory having a range of physical addresses that is greater than the range of virtual addresses (PAE36, page 3, 2nd paragraph) wherein the digital computer is programmed with a plurality of virtual-to-physical address mappings to define a plurality of virtual memory spaces, each of the plurality of virtual memory spaces includes common physical memory that is included in the other of the virtual memory spaces, and the digital computer being programmed for using the common physical memory for communication of parameters to and results from the software module (PAE36, page 3, 2nd paragraph, PAE36 discloses each process could manage a 3GB "chunk" of memory, and data could be passed between process using standard IPC or shared memory which is equivalent to common memory).

PAE36 fails to teach at least one of the virtual memory spaces includes a chunk of physical memory that is not included in any other of the plurality of virtual memory spaces. Emmes teaches at least one of the virtual memory spaces includes a chunk of physical memory that is not included in any other of the plurality of virtual memory spaces (Fig. 7A and 8; column 1, lines 9-12; column 9, lines 3-16; column 10,lines 6-

18). At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the PAE36 with Emmes. The motivation for doing so would have been an efficient resources sharing. Emmes states that "the present invention provides a way to support sharing without allocating a new band of virtual storage across all address spaces for management purposes" (column 20, lines 54-57).

Regarding claim 4, Emmes teaches a digital computer, wherein at least one other of the virtual memory spaces is directly mapped to a bottom region of the physical memory address space and is allocated to page tables (column 2, lines 1-7).

Regarding claim 5, Emmes teaches a digital computer is programmed for copying at least one parameter from a context of an application to the common physical memory, switching virtual address translation from a virtual memory space of the application to said at least one of the virtual memory spaces, executing the software module for processing said at least one parameter to produce a result placed in the common physical memory, switching the virtual address translation back to the virtual memory space of the application, and copying the result from the common physical memory to the context of the application (column 5, lines 4-27).

Regarding claims 6-7 and 16-17, Emmes teaches a digital computer, wherein the virtual memory space of the application is directly mapped to a bottom region of the physical memory address space, the digital computer is programmed for switching

virtual address translation from the virtual memory space of the application to said at least one of the virtual memory spaces by turning paging on, and the digital computer is programmed for switching virtual address translation from said at least one of the virtual memory spaces to the virtual memory space of the application by turning paging off (column 5, lines 4-27, The turning paging on and off or disabling and enabling thread scheduler are obvious features).

Regarding claims 18, PAE36 teaches a method, which includes addressing more memory space in physical memory than can be addressed by the processor in any one of the first virtual address space and the second virtual address space (PAE36, page 3, 2nd paragraph).

2. Claims 2, 3, 10, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over "PAE36 and Linux Virtual Memory System" (www.prism.gatech.edu, printed 12/5/2003), hereinafter PAE36, and Emmes (U.S. Patent 6,981,125 B2), and further in view of Atherton et al (U.S. Patent 6,081,802), hereinafter Atherton.

Regarding claim 13, PAE36 combined with Emmes teach a digital computer including at least one processor producing virtual addresses over a range of virtual addresses, a translation buffer coupled to said at least one processor for translating the virtual addresses to physical addresses, and a random access memory coupled to the translation buffer for addressing by the physical addresses and coupled to said at least

one processor for supplying data to said at least one processor (PAE36, page 3, 2nd paragraph), wherein the random access memory contains physical memory having a range of physical addresses that is greater than the range of virtual addresses, wherein the digital computer is programmed with a plurality of virtual-to-physical address mappings to define a plurality of virtual memory spaces (PAE36, page 3, 2nd paragraph), each of the plurality of virtual memory spaces includes at least one common chunk of physical memory that is included in the other of the virtual memory spaces (PAE36, page 3, 2nd paragraph, PAE36 discloses each process could manage a 3GB "chunk" of memory, and data could be passed between process using standard IPC or shared memory which is equivalent to common memory), each of the plurality of virtual memory spaces includes at least one respective separate chunk of physical memory that is not included in any other of the virtual memory spaces (Emmes, Fig. 7A and 8; column 1, lines 9-12; column 9, lines 3-16; column 10,lines 6-18), each of the respective separate chunks of physical memory is assigned for use by a respective software module, the digital computer is programmed for using the common chunk of physical memory for communication of parameters to and results from the software module, and the plurality of virtual memory spaces includes at least a first virtual memory space that is directly mapped to a bottom region of the physical memory address space, a second virtual memory space, and a third virtual memory space (PAE36, page 3, 2nd paragraph). See also, the rejection of claim 1, above.

PAE36 combined with Emmes fails to teach the common chuck of physical memory includes memory allocated to at least one processor stack, a buffer cache, BIOS, and device drivers. Atherton teaches the common chuck of physical memory includes memory allocated to at least one processor stack (column 7, lines 2-20), a buffer cache (column 13, lines 1-12), BIOS (column 7, lines 26-31), and device drivers (column 7, lines 55-59). At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the PAE36 and Emmes with Atherton. The motivation for doing so would be providing the basic interface between the computer's hardware and software resources by utilizing the operating system, in conjunction with the BIOS and associated device drivers (column 7, lines 55-59).

Regarding claim 2, Atherton teaches a digital computer, wherein the common physical memory includes physical memory allocated to a stack for said at least one processor (column 7, lines 2-20).

Regarding claims 3 and 11, Atherton teaches a digital computer, wherein each of the virtual memory spaces includes a chunk of physical memory allocated to BIOS (column 7, lines 26-31) and device drivers, the chunk of physical memory allocated to BIOS and device drivers being common to the plurality of virtual memory spaces (column 7, lines 55-59).

Regarding claim 10, Atherton teaches a digital computer, wherein the common physical memory is at the bottom of the physical address space and includes memory allocated to at least one processor stack (column 7, lines 2-20), and the respective software module assigned to the separate chunk of physical memory in the first virtual address space accesses buffer cache (column 13, lines 1-12).

3. Claims 8, 12, 14, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over "PAE36 and Linux Virtual Memory System" (www.prism.gatech.edu, printed 12/5/2003), hereinafter PAE36, and Emmes (U.S. Patent 6,981,125 B2), and Atherton et al (U.S. Patent 6,081,802), hereinafter Atherton, and further in view of Perrin et al. (U.S. Patent 6,618,792 B1), hereinafter Perrin.

Regarding claims 8, 12, 14, and 19, PAE36 combined with Emmes and Atherton teach the limitations of these claims as set forth for claims 1, 9, 13, and 15 above. However, PAE36, Emmes, or Atherton do not teach a DNLC. Perrin teaches a DNLC (column 1, lines 57-64). At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the PAE36 and Emmes with Perrin. The motivation for doing so would be to minimize read operations on the persistent storage device using a directory name look-up cache (Perrin, column 1, lines 57-64).

Regarding claim 20, Atherton teaches a method, which includes the digital computer executing snapshot copy software to access a block map in a third virtual address space (Atherton, column 13, lines 31-44).

Response to Arguments

Applicant's arguments filed 7/18/2006 have been fully considered but they are not persuasive.

Claims 1, 4-7, 9, and 15-18

Regarding claims 1, 4-7, 9, and 15-18, on page 14, second paragraph, Applicants argues that "it is not seen how this would have motivated one of ordinary skill in the art to combine and modify the fair teaching of PAE36 and Emmes to arrive at the invention of applicants".

In response, it is noted that Emmes clearly states that efficient resource sharing such as efficient virtual-to-physical address translation is one of advantages of Emmes' invention (column 20, lines 54-57). At the time of invention it would be obvious to a person of ordinary of skill in the art to combine the PAE36 with Emmes because of the above-mentioned motivation.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel B. Ko whose telephone number is 571-272-8194.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on 571-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 703-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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